REMARKS

Applicant thanks Examiner for the detailed review of the application.

Claim Rejections -35 USC § 102(b)

3. Claims 17, 20-28 and 32 are rejected under 35 U.S.C. 102(b) as being anticipated by Lawlor et al. (USPN 5,485,626, herein Lawlor).

Applicant's claim 17, includes the element, "a shared register to be **directly accessible by a second user instruction** to provide communication between the first shred and the second shred," (emphasis added). First, Lawlor specifically describes in many places that "a user cannot access it (object storage) directly at any time," (col. 7 lines16-20), a user (i.e. application program) does not have access to the object repository." (col. 11 lines 13-15), and "Objects do not "reside" in regularly addressable memory and cannot be referenced using regular instructions." Specifically, Lawlor discloses a Send/Receive Queue (SRQ), which may be accessed by a send message and a receive message. However, Lawlor specifically describes SRQ as a message queue, which is an object part of the object repository, as illustrated by Fig. 1 (msg. Qs) and described through out the disclosure. As a result, the send and receive messages are not user instructions, as Lawlor specifically discloses that no users may directly access the object storage at any time. The Office Action in fact admits that a user cannot write and execution an instruction directly to access object storage. In regard to that suggestion, applicant has amended from user-level instruction to user instruction.

Claim Rejections -35 USC § 103(a)

"The examiner bears the initial burden of factually supporting any prima facie conclusion of obviousness." MPEP § 2142. It is well established that *prima facie* obviousness is only established when three basic criteria are met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *In re Vaeck*, 947 F.2d 488 (Fed. Cir. 1991) (MPEP 2144). The Office Action has failed to meet one or more of these requirements.

The Office Action States:

16. Claims 1-12 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lawlor, in view of Galvin et al. (herein Galvin)

Applicant's claim 1 includes, "**creating in hardware without intervention of the OS**, responsive to **the non-privileged level programming instruction**, a first shared resource thread (shred) that is associated with a first private portion of a first application state, wherein the first shred and shares a second shared portion of the first application state and the first system state with at least a second shred," (claim 1 with emphasis). In general, a distinction between applicant's claim 1 and Lawlor/Galvin lies is in the **creation** of shreds by user instructions in hardware versus **dispatching or switching** between threads without OS intervention.

For example, Lawlor discloses allowing threads to access objects without the OS' thread dispatching, i.e. scheduling, process and allowing an object dispatcher to be in charge to keep operating system support to a minimum (See col 7 lines 33-42). Therefore, it is no doubt an object

of Lawlor to allow thread scheduling to occur with minimal operating system support. However, no where does Lawlor disclose "thread creation" in hardware without OS support, but rather Lawlor only focuses on efficiency of thread communication once the threads have already been created.

Similarly, Galvin does not deal with the creation of shreds in hardware without OS intervention, but rather user-thread switching without a call to the OS. Note in section 4.5.1 Thread Structure Galvin discloses, "Also, some systems implement user-level threads in user-level libraries, rather than via system calls, so thread switching does not need to call the operating system, and to cause an interrupt to the kernel." Furthermore, on page 115 Galvin discloses, "These user-level threads may be scheduled and switched among kernel-supported lightweight processes without intervention of the kernel." As can be seen, scheduling, and potentially user-thread creation, is performed through calls to libraries, not by the hardware in response to a programming instruction. Additionally, Solaris 2 operates in a P-thread style of environment, where a call to a library for creation may be made; however, the library still requires assistance from the kernel to initially create the thread. Subsequently, the libraries are capable of being utilized to schedule and switch the thread without kernel assistance and knowledge. Yet, there is a drastic difference between a hardware recognized instruction, such as part of an instruction set, that causes hardware to create and execute a thread in comparison to creation of a purely software thread utilizing a software library.

The Office Action further states:

31. Claims 35-44, 50-51, and 62-65 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lawlor and Galvin, further in view of Patterson et al. (herein Patterson).

Applicant's amended claim 35 includes, "creating, in hardware without intervention of the OS, the plurality of user-level threads of execution to be executed concurrently on multiple instruction sequencers of a processor in the machine in response to receiving the user-level programming instructions." Similar to the discussion above in reference to claim 1, Lawlor and Galvin do not disclose creation of a user-thread in hardware without intervention of the OS, but rather only context switching without intervention or creation utilizing a call to a software library. Patterson only discusses concepts of SMT generically and does not describe creation of user-level threads in hardware in response to a programming instruction without OS intervention, as in applicant's claim 35.

Claim 51 includes, "a microprocessor to implement an instruction set architecture (ISA), the microprocessor to execute multiple OS-generated threads, wherein the microprocessor is also to concurrently execute multiple shared resource threads (shreds) associated with an OS-generated thread of the multiple OS-generated threads, wherein each of the multiple shreds are associated with a private state within the OS-generated thread and a shared state of the OS-generated thread, and wherein each of the shreds is to be created utilizing hardware of the microprocessor in response to application program instructions of the ISA." In reference to the discussion above, neither Lawlor Galvin, or Patterson describe creation of threads in response to application program instructions of an ISA recognized by hardware of a microprocessor, such that a shred is created by an application program instruction of the ISA, but rather only context switching without OS intervention or

potential creation through a call to a software library.

The Office Action also states:

64. Claims 55-58 and 66 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lawlor, in view of Patterson.

Claim 55 includes, "a microprocessor, including a plurality of user-level multithreading registers, wherein the registers are addressable by one or more application program instructions to support communication among the user-level threads," (Claim 55 as amended). Similar to the discussion above in reference to claim 17, as suggested by The Office Action Lawlor explicitly discloses that object storage including state registers and counters are not addressable by user instructions, such as an application program instruction.

The Office Action also states:

74. Claims 67-71 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lawlor, further in view of Galvin.

Claim 67 includes "a third group of resources to be shared by the first shred and the second shred to hold a shared application state, wherein at least a portion of the third group of resources is to be directly accessible by a user instruction for communication between the first shred and the second shred" (claim 67 as amended). the discussion above in reference to claim 17 and 55, as suggested by The Office Action, Lawlor explicitly discloses that object storage including state registers and counters are not addressable by user instructions, such as a user instruction.

Therefore, applicant respectfully submits that independent claims 1, 17, 35, 51, 55, and 67, as well as their dependent claims, are now in condition for allowance for at least the reasons stated above. If another rejection of the claims based on the same primary references, i.e. Lawlor, Galvin, and Patterson, are to be issued, applicant respectfully requests the Examiner to contact David P. McAbee at (503) 712-4988 to setup a telephone interview in conjunction with the first listed inventor Edward T. Grochowski, whom has aided in the review of these references. If there are any additional charges, please charge Deposit Account No. 50-0221.

Respectfully submitted,
Intel Corporation

Dated: March 5, 2009

/David P. McAbee/Reg. No. 58,104
David P. McAbee
Reg. No. 58,104

Intel Corporation
M/S JF3-147
2111 NE 25th Avenue
Hillsboro, OR 97124
Tele – 503-712-4988
Fax – 503-264-1729